REMARKS

Claim 25 has been amended. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 25-30 remain pending. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 25-29 stand rejected under 35 U.S.C. § 102 as being anticipated by Wu (U.S. Patent No. 5,925,918). Claims 25-30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wei (U.S. Patent No. 5,304,504) in view of Tehrani (U.S. Patent No. 5,804,458). These rejections are respectfully traversed.

The present invention is directed at a semiconductor device. Referring to Figs. 4-9 the semiconductor device of the present invention includes a electrode stack 10 disposed upon a dielectric film 16 over a portion of a wafer, such as substrate 17. The electrode stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls 18 of the electrode stack are continuously vertical. Nitride spacers 22 extend along the continuously vertical sidewalls 18, except for the bottom portion, which may be enclosed by an oxide layer 20.

The Office Action alleges the invention is anticipated by Wu, which teaches a semiconductor device having an electrode stack 500 disposed over a dielectric film 120 on a substrate 110. See Fig. 5. However, in Wu the bottom portion of the electrode stack is a polysilicon layer 430 which is wider than the upper layers of the stack. Wu therefore, does not teach a semiconductor device having a multi-layer gate electrode stack which form continuously vertical sidewalls.

The Office Action also alleges the invention would have been obvious over the teachings of Wei and Tehrani. Referring to Fig. 4, Wei teaches a semiconductor device disposed on a dielectric film 14 over a substrate 10. Wei's semiconductor device is an electrode stack comprising polysilicon 16, refractory metal 18, and upper polysilicon 20 layers. A portion of the electrode has its sidewall in contact with oxide spacers 28. As shown in Fig. 4, the polysilicon 16 and refractory metal 18 layers of the electrode stack are wider than the upper polysilicon layer. Therefore, the electrode stack sidewalls of Wei are not continuously vertical. Similarly, in Tehrani, the semiconductor device is a stack comprising layer 20 s and wider layers 25. Thus, Tehrani also does not teach a semiconductor device with a multi-layer gate electrode stack which form continuously vertical sidewalls.

Claim 25 recites, "a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers forming continuously vertical sidewalls; and nitride spacers extending along the continuously vertical sidewalls of the gate electrode stack other than along lowermost portions of the continuously vertical sidewalls." Wu,

Wei, and Tehrani are devoid of any teachings or suggestions of a multi-layer electrode stack which form continuously vertical sidewalls and having nitride spacers which extend along the sidewalls except for the lowermost portions. Claim 25 is therefore believed to be allowable over the prior art of record. Claims 26-30 depend from claim 25 and are believed to be allowable over the prior art of record for these reasons and because the combination defined in the claims is not shown or suggested by the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

25. An integrated circuit comprising:

a semiconductor substrate [wafer];

a gate dielectric film disposed on a surface of the substrate [wafer];

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers forming continuously vertical sidewalls; and

nitride spacers extending along the continuously vertical sidewalls of the gate electrode stack other than along lowermost portions of the continuously vertical sidewalls.